NIPPON PRECISION CIRCUITS LTD.

# SM5824N

## Variable Length Static Shift Register

## OVERVIEW

The SM5824N is a 2- to 65-step variable length static shift register LSI for use in high-speed digital signal processing applications.

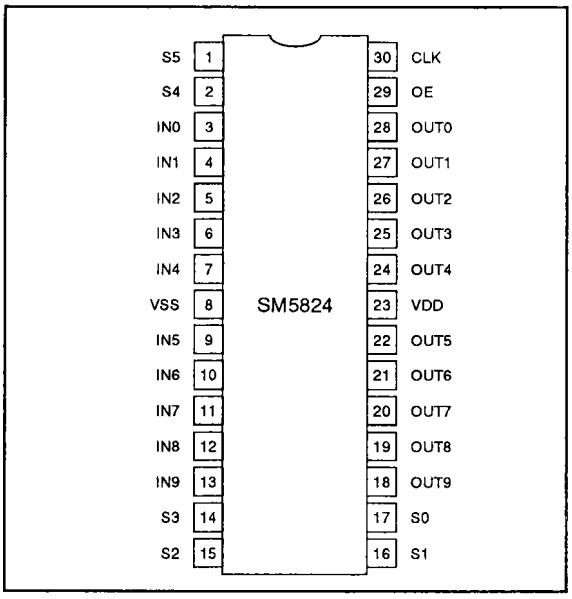
The SM5824N features tristate outputs, a 10-bit wide register and a 33.3 MHz maximum operating frequency.

The SM5824N operates from a 4.75 to 5.25 V supply and is available in 30-pin shrink DIPs.

## FEATURES

- 2- to 65-step variable shift length
- 10-bit register width
- Static register
- Tristate output
- Input pull-up resistors
- 33.3 MHz maximum operating clock frequency
- TTL-compatible inputs and outputs
- Moly-Gate® CMOS LSI
- 4.75 to 5.25 V supply voltage
- 30-pin shrink DIP

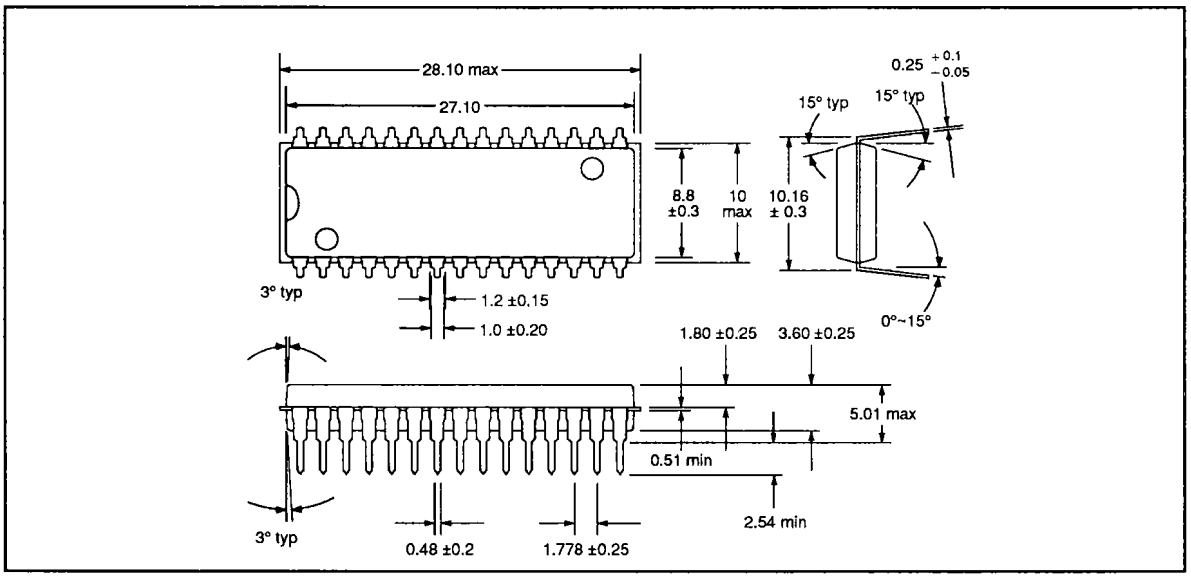
## PINOUT

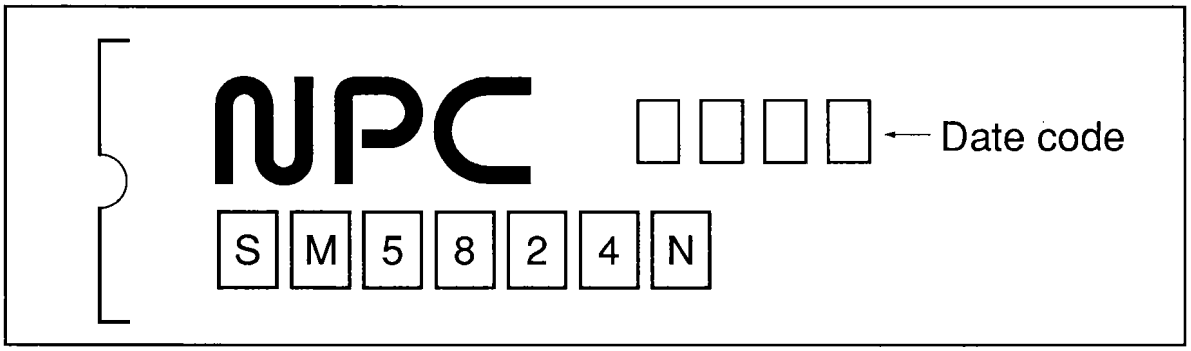


## PACKAGE DIMENSIONS AND MARKINGS

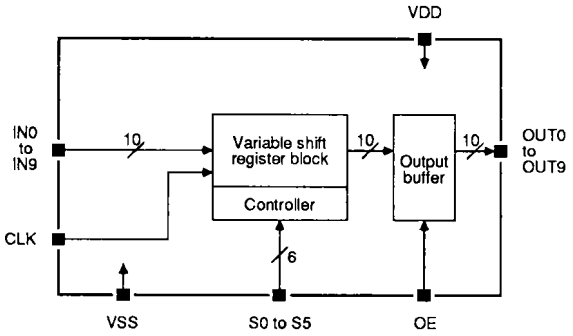
Unit : mm

### 30-pin Shrink DIP

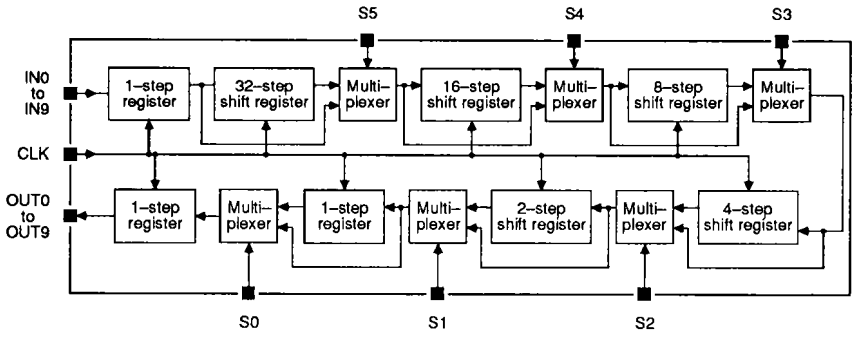


## BLOCK DIAGRAM




### Variable Shift Register Block (1 bit)




## PIN DESCRIPTION

| Number | Name | Description |
|---|---|---|
| 1 to 2 | S5 to S4 | Register length select inputs 5 (msb) to 4 |
| 3 to 7 | IN0 to IN4 | Data inputs 0 to 4 |
| 8 | VSS | Ground |
| 9 to 13 | IN5 to IN9 | Data inputs 5 to 9 |
| 14 to 17 | S3 to S0 | Register length select inputs 3 to 0 (lsb) |
| 18 to 22 | OUT9 to OUT5 | Data outputs 9 to 5 |
| 23 | VDD | Supply voltage |
| 24 to 28 | OUT4 to OUT0 | Data outputs 4 to 0 |
| 29 | OE | Output enable |
| 30 | CLK | Clock input |

**Notes**

1. All input pins have an internal pull-up resistor.
2. All output pins are tristate.

# SPECIFICATIONS

## Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{DD}$ | –0.3 to 7.0 | V |
| Input voltage range | $V_I$ | –0.3 to $V_{DD}$ + 0.3 | V |
| Power dissipation | $P_D$ | 500 | mW |
| Operating temperature range | $T_{opr}$ | –20 to 70 | deg. C |
| Storage temperature range | $T_{stg}$ | –40 to 125 | deg. C |
| Soldering temperature | $T_{SLD}$ | 255 | deg. C |
| Soldering time | $t_{SLD}$ | 10 | s |

## Recommended Operating Conditions

$T_a$ = 25 deg. C

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | 5.0 | V |
| Supply voltage range | $V_{DD}$ | 4.75 to 5.25 | V |

## Electrical Characteristics

$V_{DD}$ = 4.75 to 5.25 V, $V_{SS}$ = 0 V, $T_a$ = –20 to 70 deg. C unless otherwise noted

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Standby current consumption | $I_{DDS}$ | $V_{DD}$ = 5.25 V | – | 1 | 100 | µA |
| Operating current consumption | $I_{DD}$ | $f_{CLK}$ = 33.3 MHz, clock $V_{IL}$ = 0.5 V, clock $V_{IH}$ = 2.4 V, OE = 0 V, $V_{DD}$ = 5.0 V | – | – | 85 | mA |
| LOW-level input voltage. See note 1. | $V_{IL}$ | | – | – | 0.5 | V |
| HIGH-level input voltage. See note 1. | $V_{IH}$ | | 2.4 | – | – | V |
| LOW-level output voltage. See note 2. | $V_{OL}$ | $I_{OL}$ = 1.6 mA | – | – | 0.4 | V |
| HIGH-level output voltage. See note 2. | $V_{OH}$ | $I_{OH}$ = –0.4 mA | 2.5 | – | – | V |
| LOW-level input current. See note 1. | $I_{IL}$ | $V_I$ = 0 V | – | 10 | 20 | µA |
| HIGH-level input leakage current. See note 1. | $I_{LH}$ | $V_I$ = $V_{DD}$ | – | – | 1 | µA |
| High impedance LOW-level output leakage current. See note 2. | $I_{ZL}$ | $V_O$ = 0 V | – | – | 5 | µA |
| High impedance HIGH-level output leakage current. See note 2. | $I_{ZH}$ | $V_O$ = $V_{DD}$ | – | – | 5 | µA |

**Notes**

1. Pins IN0 to IN9, S0 to S5, OE and CLK
2. Pins OUT0 to OUT9

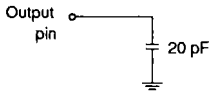
## AC Characteristics

$V_{DD}$ = 4.75 to 5.25 V, $V_{SS}$ = 0 V, $T_a$ = −20 to 70 deg. C

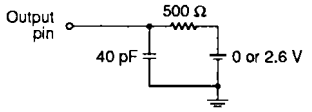
| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Clock frequency | $f_{CLK}$ | $V_{IL}$ = 0.5 V, $V_{IH}$ = 2.4 V | – | – | 33.3 | MHz |
| Clock rise and fall time | $t_{CR}$, $t_{CF}$ | | – | – | 100 | ns |
| Clock LOW- and HIGH-level pulsewidth | $t_{WL}$, $t_{WH}$ | | 13 | – | – | ns |
| IN0 to IN9 input setup time | $t_{S1}$ | | 13 | – | – | ns |
| S0 to S5 input setup time | $t_{S2}$ | | 50 | – | – | ns |
| IN0 to IN9 input hold time | $t_{H1}$ | | 0 | – | – | ns |
| S0 to S5 input hold time | $t_{H2}$ | | 5 | – | – | ns |
| CLK to (OUT0 to OUT9) propagation delay | $t_{PD}$ | See note 1. | – | – | 28 | ns |
| CLK to (OUT0 to OUT9) data hold time | $t_{OH}$ | See note 1. | 10 | – | – | ns |
| OE to (OUT0 to OUT9) output enable delay | $t_{OEN}$ | See note 2. | – | – | 25 | ns |
| OE to (OUT0 to OUT9) output disable delay | $t_{ODE}$ | See note 2. | – | – | 25 | ns |
| Input capacitance. See note 3. | $C_I$ | f = 1 MHz | – | – | 10 | pF |
| Output capacitance. See note 4. | $C_O$ | f = 1 MHz, OE = 0 V | – | – | 20 | pF |

**Notes**

1. Measured under the load conditions shown in the following figure.

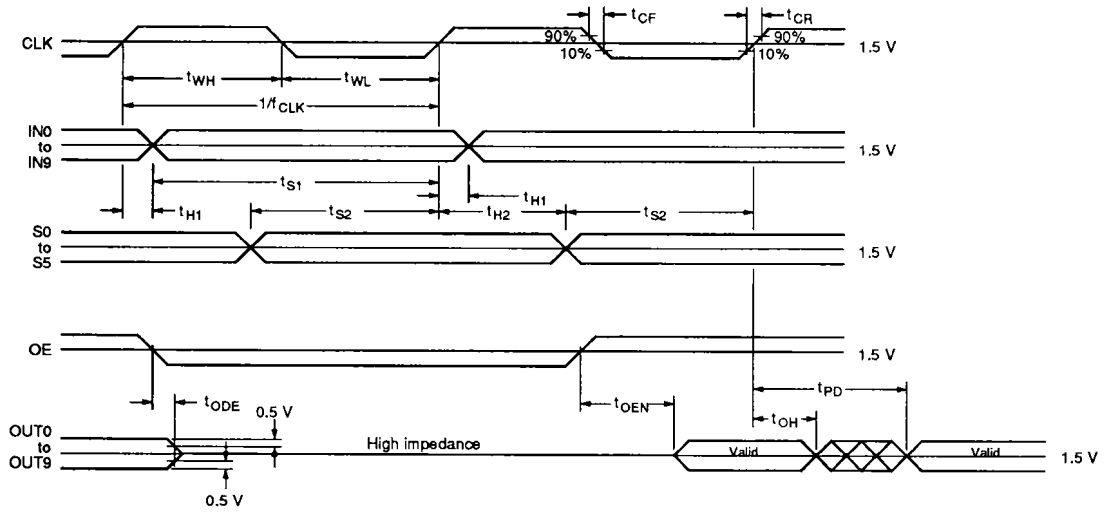



2. Measured under the load conditions shown in the following figure.




3. Pins IN0 to IN9, S0 to S5, OE and CLK
4. Pins OUT0 to OUT9

## AC timing




# FUNCTIONAL DESCRIPTION

## Register Length Selection

The shift register length is selected by the register length select inputs, S0 to S5, according to the following equation.

$$L = 32 \cdot (S5) + 16 \cdot (S4) + 8 \cdot (S3) + 4 \cdot (S2) + 2 \cdot (S1) + (S0) + 2$$

where a HIGH level has value 1 and a LOW level has value 0. Only LOW levels need to be set, because the inputs have pull-up resistors.

Table 1. Shift register lengths

| Length | S5 | S4 | S3 | S2 | S1 | S0 |
|---|---|---|---|---|---|---|
| 65 | 1 | 1 | 1 | 1 | 1 | 1 |
| 64 | 1 | 1 | 1 | 1 | 1 | 0 |
| 63 | 1 | 1 | 1 | 1 | 0 | 1 |
| 62 | 1 | 1 | 1 | 1 | 0 | 0 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 35 | 1 | 0 | 0 | 0 | 0 | 1 |
| 34 | 1 | 0 | 0 | 0 | 0 | 0 |
| 33 | 0 | 1 | 1 | 1 | 1 | 1 |
| 32 | 0 | 1 | 1 | 1 | 1 | 0 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 4 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 |

## Tristate Output Control

When OE is LOW, the data outputs OUT0 to OUT9 are high impedance. When OE is HIGH, they are enabled. The state of CLK does not affect the outputs.